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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,626	10/29/2003	Bala Ramachandran	03SKY0003	5553

24504 7590 03/18/2008
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ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
03/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Arguments

1. Applicant's arguments filed 11/24/2008 have been fully considered but they are not persuasive.

   a. Regarding **claims 1,11,21**, the applicant contends Yan et al fails to disclose the limitation "selectively DC-offset correcting comprises selecting ... different DC-offset correcting bandwidths based on which system baseband signal is to be processed." The examiner respectfully disagrees. Yan discloses "The DC offset correction operates to force the DC levels of the differential in-phase signals I+ and I- to a common level and the DC levels of the differential quadrature signals Q+ and Q- to a common level to reduce or eliminate distortion caused by having a DC offset between the respective differential signals." Depending on the offset of the input baseband signal as shown in Fig. 1, labels I+, I-, Q+ and Q-, the DC correction signal would perform an adjustment to provide a common level between Q+, Q- and I+, I-. In implementation, it is implied that the DC correction circuitry will perform a selection or choice in order to determine the amount of adjustment, depending on the baseband signal inputted, needed to provide a common level as discussed in the prior art. Thus, Yan discloses the recited limitation.

   The applicant further contends "Yan does not appear to be responsive in any way to the system baseband signal that is to be processed." The examiner respectfully disagrees. The examiner would like to point to Fig. 1, wherein the received signal is adjusted based on the system in which the signal was transmitter. Labels 38a-d and 40a-d show that the signal is being filtered and amplified based on the system type. The DC offset

correction is performed in label 56, where the signal received by label 56 is processed based on the type of system in which the signal was received. Thus, the DC offset correction circuit will perform adjustments based on the type of the system since the input signal is previously processed based on the type of system.

The applicant further contends "It is not taught, disclosed or suggested in Yan that the DC-offset element (which is distinct from the dummy LNA) is bandwidth switchable." The examiner respectfully disagrees. Yan discloses "The DC offset correction operates to force the DC levels of the differential in-phase signals I+ and I- to a common level and the DC levels of the differential quadrature signals Q+ and Q- to a common level to reduce or eliminate distortion caused by having a DC offset between the respective differential signals." Depending on the offset of the input baseband signal as shown in Fig. 1, labels I+, I-, Q+ and Q-, the DC correction signal would perform an adjustment to provide a common level between Q+, Q- and I+, I-. In implementation, it is implied that the DC correction circuitry will perform a selection or choice in order to determine the amount of adjustment, depending on the baseband signal inputted, needed to provide a common level as discussed in the prior art. Thus, Yan discloses the recited limitation. As previously indicated, the DC correction circuit will perform a selection or choice in order to determine the amount of adjustment. The examiner would like to point to Fig. 1. Fig. 1 of Yan et al shows that the LNAs process the received signal based on the system type. The output from the LNAs would have different bandwidths depending on the system type in which the signal was transmitted. Col. 6, lines 39-60 discloses

"These differential output signal of the LNAs 40A-E result in DC offsets in the differential in-phase and quadrature signals I+, I-, Q+ and Q- due to the mixing action with the LO signal in the down-conversion circuitry. Thus the control system 32 activates the DC correction circuitry 56 to monitor the levels of the differential in-phase and quadrature signals I+, I-, Q+ and Q- and provide any necessary DC offset correction (step 110)." Since the LNA affects the input to the DC offset correction, the correction will occur within the bandwidth of the signal outputted by the LNA depending on the type of system in which the signal received was transmitted. Thus, the DC offset correction will perform switchable bandwidths depending on the type of system and the output of the LNAs. Furthermore, the amount or bandwidth in which DC offset correction will occur depends on the shift between the I and Q from the center of the I and Q plane. Depending on the input signal to the DC offset correction circuit, the bandwidth or amount needed to adjust the DC offset must be determined or selected or switched given the mode of the system in which the received signal is transmitted. Thus, when Yan discloses adjusting the I and Q in positive and negative direction, the total adjustment in the positive and negative direction of I and Q would depend on the amount or bandwidth needed to center the signal within the I and Q plane. Thus, Yan discloses "switchable bandwidth" or "selectable DC offset correction".

b. Regarding **claims 2-10,12-20,22-27,29,31,32,33** such claims depend on independent claims 1,11,21. Please refer to the rebuttal of claims 1,11, and 21, respectively.

c. Regarding **claims 6,7,10,15,17 and 19**, the applicant traverses that filtering that it is well known in the art that filtering can be low pass, all pass or FIR "since such filters

are well known in the art and can be used to perform the functionality of filtering, wherein the filter is chosen based on the inventor's choice and which would produce the output as desired by the inventor." The examiner respectfully disagrees. To prove the examiner's The examiner is providing a document indicating types of filtering systems that are well known in the art. Please refer to the reference, "Digital Filter Terminology". Note the reference above is not being used as part of the rejection. The reference is used to prove the examiner's point of view.

d. Regarding **claims 9,18,26,** the applicant contends the limitations "wherein the processing includes sampling at a first sampling rate for the first baseband signal and a second sampling rate for the second baseband signal" is inadequately addressed. The examiner respectfully disagrees. Yan discloses processing the received signal depending on a mode as shown in Fig.1. The down conversion is performed to convert the signal to baseband signal. (Col. 1, lines 60-65) Down conversion is adjusted by the frequency synthesizer as shown in Fig. 1. label 34. In order to down convert appropriately, Nyquist must be considered. Due to the limitations of Nyquist and the frequency of the mode of the system in which the received signal is transmitted (Col. 1, lines 11-33 discusses the different frequency range used for different system modes.), down conversion must provide different sampling rates (first and second sampling rates) to provide a baseband signals (first and second baseband signals).

e. Regarding **claims 28-33** rejected based on the 1st prior art rejection, the applicant contends Peterzell fails to disclose "a direct current (DC) correction element configured to include switchable bandwidths." The examiner respectfully disagrees. The examiner

would like to point to Fig. 3, wherein the received signal is filtered and adjusted based on the mode or type of the system. The DC offset correction is performed on the input signal depending on the type of system in which the received signal is transmitted. The amount of DC offset found would depend on the LO I and Q mixers as disclosed by Peterzell. Since the input signal depends on the system mode, the amount of adjustment would depend on the LO's affect on the signal. LO will affect the received signal in different ways, since the signal received is adjusted prior to DC offset correction depending on the mode of the system. Thus, the amount of adjustment or bandwidth of the DC offset correction needed would depend on the system mode of the signal, and the affect of the LO on the signal.

f. Regarding **claims 28-33** rejected based on the 2nd prior art rejection, the applicant contends Yan fails to teach "the common level to which the offset corrector forces the signals has any bearing on the bandwidth of the DC correction elements." Such assertion lies in the previous assertion that Yan fails to teach "switchable bandwidths" for DC offset correction. Such assertion has been addressed above in the rebuttal of claims 1,11 and 21. Please refer to the rebuttal above.

The applicant further contends Yan fails to disclose the limitation "wherein ... selectively DC-offset correcting comprises selecting different DC-offset correcting bandwidths based on which system baseband signal is to be processed". Such assertion has been addressed above in the rebuttal of claims 1,11 and 21. Please refer to the rebuttal above.

The applicant further contends Yan fails to disclose DC offset correction involves " switch[ing] the bandwidth of the DC-offset correcting elements." Such assertion has been addressed above in the rebuttal of claims 1,11 and 21. Please refer to the rebuttal above.

/David C. Payne/

Supervisory Patent Examiner, Art Unit 2611